

	L #	Hits	Search Text	DBs
1	L1	19226	(instruction prefetch\$3 fetch\$3) near10 (buffer queue)	USPAT; US-PPGPUB
2	L2	53755	(combin\$3 complex) near5 (operation instruction)	USPAT; US-PPGPUB
3	L4	6994	(instruction prefetch\$3 fetch\$3) near10 (buffer queue)	EPO; JPO; DERWENT; IBM_TDB
4	L5	11748	(combin\$3 complex) near5 (operation instruction)	EPO; JPO; DERWENT; IBM_TDB
5	L3	201	1 near30 2	USPAT; US-PPGPUB
6	L6	16	4 near50 5	EPO; JPO; DERWENT; IBM_TDB
7	L9	202	1 near99 2	USPAT; US-PPGPUB
8	L10	16	4 near99 5	EPO; JPO; DERWENT; IBM_TDB
9	L12	3627	(merg\$3) near5 (operation instruction)	USPAT; US-PPGPUB
10	L14	515	(merg\$3) near5 (operation instruction)	EPO; JPO; DERWENT; IBM_TDB
11	L15	7	4 near50 14	EPO; JPO; DERWENT; IBM_TDB
12	L13	87	1 near30 12	USPAT; US-PPGPUB
13	L16	87	1 near99 12	USPAT; US-PPGPUB

	Document ID	U	Title	Current OR
1	US 20030 07454 2 A1	<input type="checkbox"/>	Multiprocessor system and program optimizing method	712/20
2	US 20030 05317 0 A1	<input type="checkbox"/>	Optoelectronic device capable of participating in in-band traffic	398/139
3	US 20020 11439 5 A1	<input type="checkbox"/>	SYSTEM METHOD AND APPARATUS FOR A MOTION COMPENSATION INSTRUCTION GENERATOR	375/240 .18
4	US 20020 08780 6 A1	<input type="checkbox"/>	Cache coherence protocol engine and method for efficient processing of interleaved memory transactions in a multiprocessor system	711/141
5	US 20020 07828 5 A1	<input type="checkbox"/>	Reduction of interrupts in remote procedure calls	710/260
6	US 20020 05744 6 A1	<input type="checkbox"/>	MULTI- INSTRUCTION STREAM PROCESSOR	358/1.1 3
7	US 20020 05099 2 A1	<input type="checkbox"/>	Geometry instructions for graphics data compression	345/423
8	US 20020 03425 2 A1	<input type="checkbox"/>	System, method and apparatus for an instruction driven digital video processor	375/240 .17
9	US 20010 05068 2 A1	<input type="checkbox"/>	Decompression of variable-length encoded compressed three-dimensional graphics data	345/420
10	US 20010 02197 1 A1	<input type="checkbox"/>	SYSTEM FOR EXECUTING INSTRUCTIONS HAVING FLAG FOR INDICATING DIRECT OR INDIRECT SPECIFICATION OF A LENGTH OF OPERAND DATA	712/215
11	US 66752 87 B1	<input type="checkbox"/>	Method and apparatus for store forwarding using a response buffer data path in a write-allocate-configurable microprocessor	712/216
12	US 66745 36 B2	<input type="checkbox"/>	Multi-instruction stream processor	358/1.1 5
13	US 66437 45 B1	<input type="checkbox"/>	Method and apparatus for prefetching data into cache	711/138
14	US 66222 18 B2	<input type="checkbox"/>	Cache coherence protocol engine and method for efficient processing of interleaved memory transactions in a multiprocessor system	711/141
15	US 66034 70 B1	<input type="checkbox"/>	Compression of surface normals in three-dimensional graphics data	345/419
16	US 65320 12 B2	<input type="checkbox"/>	Geometry instructions for graphics data compression	345/423
17	US 65257 22 B1	<input type="checkbox"/>	Geometry compression for regular and irregular mesh structures	345/419
18	US 65223 27 B2	<input type="checkbox"/>	Decompression of variable-length encoded compressed three-dimensional graphics data	345/428
19	US 65223 26 B1	<input type="checkbox"/>	Decompression of quantized compressed three-dimensional graphics data	345/427

	Document ID	U	Title	Current OR
20	US 65078 98 B1	<input type="checkbox"/>	Reconfigurable data cache controller	711/168
21	US 64903 24 B1	<input type="checkbox"/>	System, method and apparatus for a variable output video decoder	375/240 .25
22	US 64776 40 B1	<input type="checkbox"/>	Apparatus and method for predicting multiple branches and performing out-of-order branch resolution	712/238
23	US 64635 25 B1	<input type="checkbox"/>	Merging single precision floating point operands	712/222
24	US 64216 96 B1	<input type="checkbox"/>	System and method for high speed execution of Fast Fourier Transforms utilizing SIMD instructions on a general purpose processor	708/404
25	US 64149 96 B1	<input type="checkbox"/>	System, method and apparatus for an instruction driven digital video processor	375/240 .17
26	US 64146 87 B1	<input type="checkbox"/>	Register setting-micro programming system	345/503
27	US 63965 04 B1	<input type="checkbox"/>	Graphical image data reformatting method and apparatus	345/589
28	US 63935 49 B1	<input type="checkbox"/>	Instruction alignment unit for routing variable byte-length instructions	712/204
29	US 63935 45 B1	<input type="checkbox"/>	Method apparatus and system for managing virtual memory with virtual-physical mapping	712/34
30	US 63518 01 B1	<input type="checkbox"/>	Program counter update mechanism	712/205
31	US 63493 79 B1	<input type="checkbox"/>	System for executing instructions having flag for indicating direct or indirect specification of a length of operand data	712/210
32	US 63361 80 B1	<input type="checkbox"/>	Method, apparatus and system for managing virtual memory with virtual-physical mapping	712/34
33	US 63361 68 B1	<input type="checkbox"/>	System and method for merging multiple outstanding load miss instructions	711/141
34	US 63213 03 B1	<input type="checkbox"/>	Dynamically modifying queued transactions in a cache memory system	711/140
35	US 63112 58 B1	<input type="checkbox"/>	Data buffer apparatus and method for storing graphical data using data encoders and decoders	711/200
36	US 63112 54 B1	<input type="checkbox"/>	Multiple store miss handling in a cache memory memory system	711/126
37	US 63075 57 B1	<input type="checkbox"/>	Decompression of three-dimensional graphics data including quantization, delta-encoding, and variable-length encoding	345/428
38	US 62891 38 B1	<input type="checkbox"/>	General image processor	382/307
39	US 62759 21 B1	<input type="checkbox"/>	Data processing device to compress and decompress VLIW instructions by selectively storing non-branch NOP instructions	712/24
40	US 62726 24 B1	<input type="checkbox"/>	Method and apparatus for predicting multiple conditional branches	712/239
41	US 62722 57 B1	<input type="checkbox"/>	Decoder of variable length codes	382/246
42	US 62694 27 B1	<input type="checkbox"/>	Multiple load miss handling in a cache memory system	711/140

	Document ID	U	Title	Current OR
43	US 62594 56 B1	<input type="checkbox"/>	Data normalization techniques	345/619
44	US 62463 96 B1	<input type="checkbox"/>	Cached color conversion method and apparatus	345/604
45	US 62398 05 B1	<input type="checkbox"/>	Method and apparatus for geometric compression of three-dimensional graphics data	345/419
46	US 62370 85 B1	<input type="checkbox"/>	Processor and method for generating less than (LT), Greater than (GT), and equal to (EQ) condition code bits concurrent with a logical or complex operation	712/223
47	US 62370 83 B1	<input type="checkbox"/>	Microprocessor including multiple register files mapped to the same logical storage and inhibiting synchronization between the register files responsive to inclusion of an instruction in an instruction sequence	712/217
48	US 62370 79 B1	<input type="checkbox"/>	Coprocessor interface having pending instructions queue and clean-up queue and dynamically allocating memory	712/34
49	US 61956 74 B1	<input type="checkbox"/>	Fast DCT apparatus	708/402
50	US 61579 98 A	<input type="checkbox"/>	Method for performing branch prediction and resolution of two or more branch instructions within two or more branch prediction buffers	712/238
51	US 61417 34 A	<input type="checkbox"/>	Method and apparatus for optimizing the performance of LDxL and STxC interlock instructions in the context of a write invalidate protocol	711/144
52	US 61187 24 A	<input type="checkbox"/>	Memory controller architecture	365/230 .05
53	US 60880 34 A	<input type="checkbox"/>	Decompression of surface normals in three-dimensional graphics data	345/420
54	US 60617 49 A	<input type="checkbox"/>	Transformation of a first dataword received from a FIFO into an input register and subsequent dataword from the FIFO into a normalized output dataword	710/65
55	US 60493 90 A	<input type="checkbox"/>	Compressed merging of raster images for high speed digital printing	358/1.1 5
56	US 60473 69 A	<input type="checkbox"/>	Flag renaming and flag masks within register alias table	712/217
57	US 60353 90 A	<input type="checkbox"/>	Method and apparatus for generating and logically combining less than (LT), greater than (GT), and equal to (EQ) condition code bits concurrently with the execution of an arithmetic or logical operation	712/220
58	US 60353 87 A	<input type="checkbox"/>	System for packing variable length instructions into fixed length blocks with indications of instruction beginning, ending, and offset within block	712/210
59	US 60353 86 A	<input type="checkbox"/>	Program counter update mechanism	712/205
60	US 60286 10 A	<input type="checkbox"/>	Geometry instructions for decompression of three-dimensional graphics data	345/501
61	US 59481 00 A	<input type="checkbox"/>	Branch prediction and fetch mechanism for variable length instruction, superscalar pipelined processor	712/238
62	US 59331 53 A	<input type="checkbox"/>	Mesh buffer for decompression of compressed three-dimensional graphics data	345/501
63	US 59055 02 A	<input type="checkbox"/>	Compression of three-dimensional graphics data using a generalized triangle mesh format utilizing a mesh buffer	345/420
64	US 58700 94 A	<input type="checkbox"/>	System and method for transferring compressed three-dimensional graphics data	345/419

	Document ID	U	Title	Current OR
65	US 58671 67 A	<input type="checkbox"/>	Compression of three-dimensional graphics data including quantization, delta-encoding, and variable-length encoding	345/419
66	US 58601 07 A	<input type="checkbox"/>	Processor and method for store gathering through merged store operations	711/140
67	US 58549 13 A	<input type="checkbox"/>	Microprocessor with an architecture mode control capable of supporting extensions of two distinct instruction-set architectures	712/210
68	US 58420 04 A	<input type="checkbox"/>	Method and apparatus for decompression of compressed geometric three-dimensional graphics data	345/501
69	US 58058 78 A	<input type="checkbox"/>	Method and apparatus for generating branch predictions for multiple branch instructions indexed by a single instruction pointer	712/239
70	US 57991 62 A	<input type="checkbox"/>	Program counter update mechanism	712/205
71	US 57933 71 A	<input type="checkbox"/>	Method and apparatus for geometric compression of three-dimensional graphics data	345/418
72	US 57489 32 A	<input type="checkbox"/>	Cache memory system for dynamically altering single cache memory line as either branch target entry or prefetch instruction queue based upon instruction sequence	715/526
73	US 56597 33 A	<input type="checkbox"/>	Sort processing method and apparatus for sorting data blocks using work buffer merge data records while sequentially transferring data records from work buffers	707/7
74	US 55599 75 A	<input type="checkbox"/>	Program counter update mechanism	712/230
75	US 52689 95 A	<input type="checkbox"/>	Method for executing graphics Z-compare and pixel merge instructions in a data processor	345/422
76	US 52300 68 A	<input type="checkbox"/>	Cache memory system for dynamically altering single cache memory line as either branch target entry or pre-fetch instruction queue based upon instruction sequence	711/137
77	US 52029 72 A	<input type="checkbox"/>	Store buffer apparatus in a multiprocessor system	711/123
78	US 51971 45 A	<input type="checkbox"/>	Buffer storage system using parallel buffer storage units and move-out buffer registers	711/143
79	US 51670 26 A	<input type="checkbox"/>	Simultaneously or sequentially decoding multiple specifiers of a variable length pipeline instruction based on detection of modified value of specifier registers	712/210
80	US 51573 88 A	<input type="checkbox"/>	Method and apparatus for graphics data interpolation	345/673
81	US 51485 28 A	<input type="checkbox"/>	Method and apparatus for simultaneously decoding three operands in a variable length instruction when one of the operands is also of variable length	712/210
82	US 51426 33 A	<input type="checkbox"/>	Preprocessing implied specifiers in a pipelined processor	712/225
83	US 51135 15 A	<input type="checkbox"/>	Virtual instruction cache system using length responsive decoded instruction shifting and merging with prefetch buffer outputs to fill instruction buffer	711/125
84	US 50816 98 A	<input type="checkbox"/>	Method and apparatus for graphics display data manipulation	345/422
85	US 48902 20 A	<input type="checkbox"/>	Vector processing apparatus for incrementing indices of vector operands of different length according to arithmetic operation results	712/8
86	US 46384 29 A	<input type="checkbox"/>	Data processing apparatus for processing operand store conflict	712/218
87	US 44970 23 A	<input type="checkbox"/>	Linked list of timed and untimed commands	712/205

	Docum ent ID	U	Title	Current OR
1	JP 06290 208 A	<input type="checkbox"/>	VECTOR PROCESSOR	
2	JP 05197 609 A	<input type="checkbox"/>	STORE BUFFER MANAGING SYSTEM	
3	JP 04112 328 A	<input type="checkbox"/>	DEGENERATION CONTROL SYSTEM FOR STORE INSTRUCTION	
4	JP 02156 349 A	<input type="checkbox"/>	MEMORY CONTROLLER	
5	EP 99289 3 A	<input type="checkbox"/>	Processor for executing instructions in parallel has instruction buffer and decoders storing and decoding two instructions and arbitration and merge logic arbitrating between instructions	
6	US 52689 95-A	<input type="checkbox"/>	Executing method for graphics Z-compare and pixel merge instructions in data processor - involves using pixel compare result_vector_to_selectively_store_pixels_in_image-buffer according to pixel merge instruction	
7	US 52300 68 A	<input type="checkbox"/>	Integrated instruction-queue and branch-target cache memory - has up to three active instruction queues each associated with sequential instruction stream started by control transfer instruction	